54F/74F259

8-Bit Addressable Latch

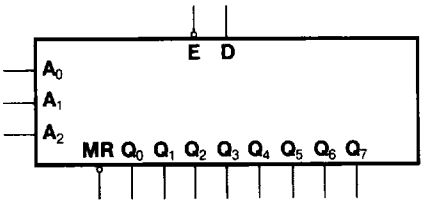
Description

The 'F259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

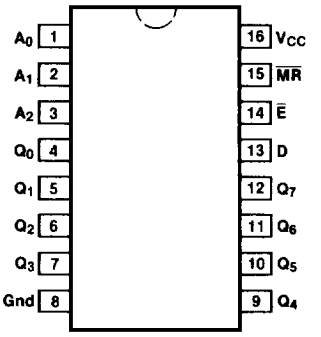
- **Serial-to-Parallel Conversion**
- **Eight Bits of Storage with Output of Each Bit Available**
- **Random (Addressable) Data Entry**
- **Active High Demultiplexing or Decoding Capability**
- **Easily Expandable**
- **Common Clear**

Ordering Code: See Section 5

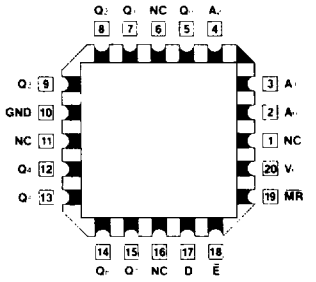
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

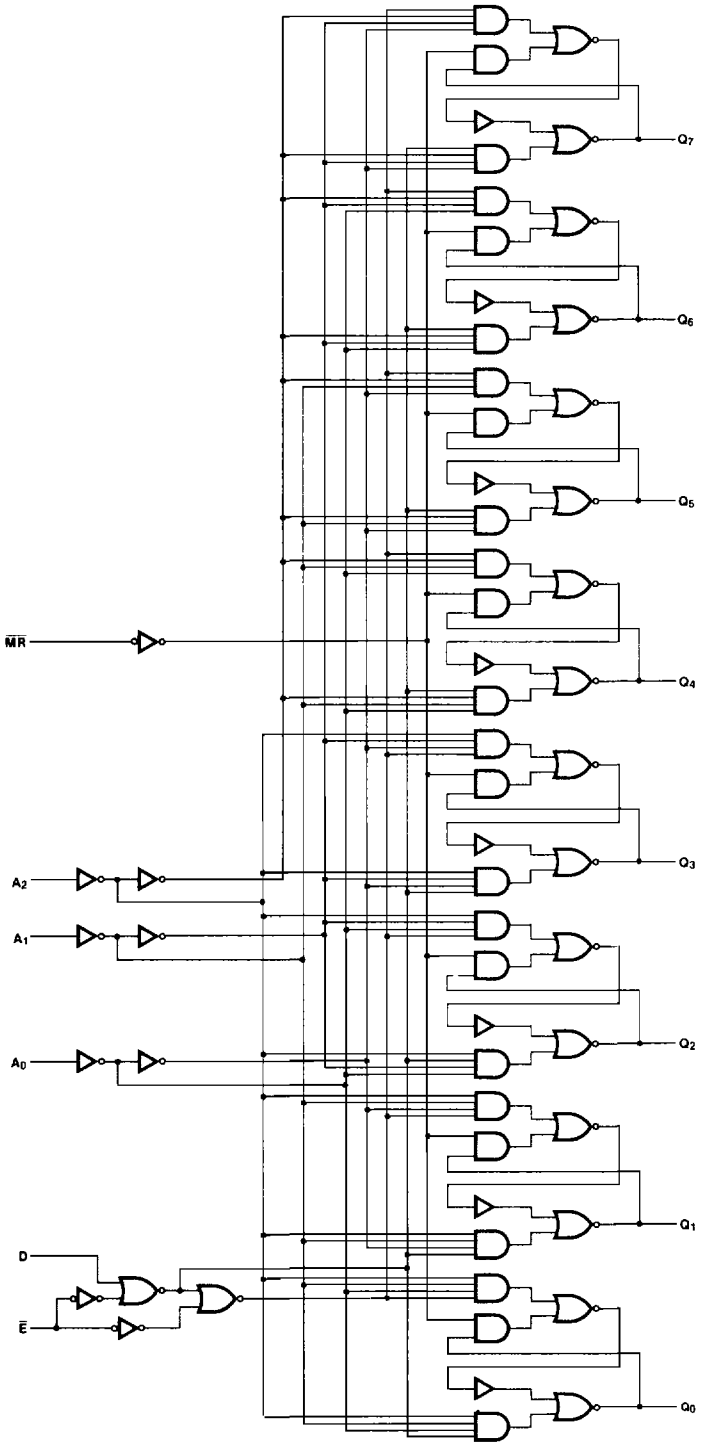


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Address Inputs	0.5/0.375
D	Data Input	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	1.0/0.75
$\overline{MR}$	Master Reset (Active LOW)	0.5/0.375
Q_0-Q_7	Latch Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'F259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 'F259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the 'F259.

Mode Select-Function Table

Operating Mode	Inputs													
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (Do Nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable Latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Mode Select Table

$\overline{E}$	$\overline{MR}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			40	mA	Output HIGH	V_{CC} = Max
I_{CCL}				75		Output LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		10.5 7.0						ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		9.0 6.5						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		13.0 9.0						ns	3-1 3-10
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		9.0						ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D to $\overline{E}$	4.0 4.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to $\overline{E}$	1.0 1.0				
$t_s(L)$	Setup Time, LOW Address to Enable[a]	4.0			ns	3-16
$t_h(H)$	Hold Time, HIGH Address to Enable[b]	0				
$t_w(H)$ $t_w(L)$	$\overline{E}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-8
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-11

Notes

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.